Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended and new claims added to better clarify Applicants claimed invention.

Support for the new claims is found in the original claims and/or Specification. No new matter has been entered.

For example, support for limitations in claims 1 and 11 are found in the original claim and in the Specification. See for example:

Paragraph 0034, beginning on page 18:

"Referring to Figure 2, exemplary cathode contact areas 202 are shown surrounding **a periphery portion 204 (exclusion region)** of a semiconductor wafer 200. Inside the periphery portion 204 of the semiconductor wafer is a **central portion 206 including active device areas**. Preferably the cathode contact areas 202 are located at the periphery portion 204 of the semiconductor wafer 200 to include the entire circumference of the semiconductor wafer 200."

And paragraph 0027 beginning on page 13:

"Further, the semiconductor wafer may consist of several active device areas forming **individual chips located in a central portion of the wafer.**"

Claim Rejections under 35 USC 103(a)

1. Claims 1-5, 7-16 and 18-20 stand rejected under 35 USC 103(a) as being unpatentable over Landau (6,261,433) in view of Palagonia (5,907,785) and Romankiw (6,596, 624).

Landau discloses and teaches a method for achieving reliable electroplating onto semiconductor substrates (see Abstract). IN the discussion in the Background of the Invention Landau discusses the prior art of electroplating semiconductor circuitry wiring including dual damascenes. Landau's discussion of the prior art is consistent with Applicants discussion of the prior art for forming metal interconnects. Landau additionally discloses cathode contacts used for applying a current to the semiconductor plating surface which Landau teaches are **in contact with a metal seed layer** "as close as practically possible to the edge of the substrate" (col 3, lines 45-52). Landau teaches an excluded area at the periphery can no longer be used to form devices on the substrate (col 3, lines 51-52).

Landau discloses nothing else concerning a cathode contact area other than that contact pins contact a conductive layer (metal seed layer) positioned near the edge of the substrate (col 6, lines 53 to 57). Landau therefore does not disclose, discuss or suggest cathode contact areas at the periphery of the wafer disposed in an **exclusion region** or their formation as disclosed and claimed by Applicants. Rather, Landau specifically teaches away from Applicants disclosed and claimed invention by teaching that no devices are formed in the "excluded area" at the periphery.

Furthermore, with respect to claim 11 and claim 21 Landau teaches away from Applicants disclosed and claimed invention:

e.g., in claim 11:

"forming a metal layer over the electrically conductive pathway surfaces to form a plurality of contact pads for contacting a cathode for carrying out an electroplating process on a central portion of the semiconductor wafer comprising a damascene structure and a metal seed layer in electrical communication with the conductive layer."

Applicants "conductive layer" refers to a conductive layer underlying the contact pads and an insulating layer. See also

claim 21. Rather, Landau teaches that electrical (cathode) contact to the substrate (semiconductor wafer) for carry out an electroplating process is made directly to a metal seed layer formed as close to the edge as practicable (see, e.g., col 3, lines 45-52), e.g., exclusion area.

Other than supporting Applicants characterization of the state of the prior art, Landau is largely irrelevant to Applicants disclosed and claimed invention, but rather directly teaches away from Applicants disclosed and claimed invention. Applicants further respectfully suggest that Examiners characterization of the disclosure of Landau is mistaken. For example, Examiner asserts that "The formation of metallization structures occurs across the width of the wafer. The via openings adjacent the periphery of the wafer may be considered to correspond to cathode contact area etched openings recited in claim 1." Examiner provides no factual basis for the foregoing assertions, and indeed, such assertions are inconsistent with the teachings of Landau who specifically teaches an "excluded area", at the wafer periphery where active device portions (e.g., damascene structures) are excluded, consistent with Applicants characterization of the state of the prior art (i.e., exclusion area).

"Finally, the prior art reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

The fact that Palagonia discloses the formation of contact pads does not help Examiner in establishing a *prima facie* case of obviousness. Palagonia teaches forming raised contact pads on individual die (see col 2, lines 32-44) "within the perimeter established by the sides of the chips" (col 3, lines 40-41). It is well known in the art that die are not formed in an exclusion area at the periphery (edge) of a process wafer as taught by Landau and Applicants Specification. Moreover, there is no apparent motive for combining Palagonia with Landau, since Landau

does not suggest the usefulness of contact pads at the wafer periphery (edge) for making electrical contact with a metal seed layer. Such contact pads would add nothing to the method and apparatus of Landau, and since taught by Palagonia to be formed within the die perimeter, would change the principal of operation of Landau of making contact with the metal seed layer at the wafer edge by contact pins. Nevertheless, such combination of Palagonia with Landau does not produce Applicants disclosed and claimed invention.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)*.

Romankiw discloses "a multilayer integrated circuit structure joined to a chip carrier, and a process of making, in which the area normally occupied by a solid dielectric material in the IC is at least partially hollow" (see Abstract). To provide mechanical support for the partially hollow IC, Romankiw teaches forming "dummy columns" strategically placed uniformly

throughout **the chip** and in the **chip periphery**" (see col 5, lines 16-23).

There is no apparent motivation for combining Romankiw with Landau. Romankiw does not teach or discuss an electrodeposition process as is taught by Landau. Palagonia and Romankiw disclose contact pads for mounting chips to subsequent boards or higher levels of assembly. The contact pads of either Palagonia or Romankiw would not be expected to work with the electrodeposition process of Landau who teaches cathode contact pins making contact with a metal seed layer at the edge of the wafer, e.g., in an exclusion area where no devices (e.g., chips are formed). Moreover, combining Romankiw with Palagonia and Landau does not produce Applicants claimed invention.

"Applicants point out that "we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).*

2. Claims 6 and 17 stand rejected under 35 USC 103(a) as being unpatentable over Landau (6,261,433) in view of Palagonia

(5,907,785) and Romankiw (6,596, 624), above, and further in view of Krishnamoorthy et al. (6,319,387).

Applicants reiterate the above comments with respect to Landau Palagonia and Romankiw. The fact that Krishnamoorthy et al. discloses an equation supporting the teaching that a low-K dielectric material should be used in the manufacture of high performance integrated circuits (see col 1, line 60 - col 2, line 9) to minimize capacitance does not help Examiner in establishing a *prima facie* case of obviousness with respect to Applicants disclosed and claimed invention.

Since Examiner has not established a *prima facie* case of obviousness with respect to the independent claims, neither has one been shown for the dependent claims.

The Claims have amended and new claims added to clarify Applicants claimed invention. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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